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A Single-Switch Improved Valley-Fill Passive Current Shaper for Compact Fluorescent Lightings

G.Ramakrishnaprabu¹, Gunasekar²

Associate Professor, Department of EEE, VMKV Engineering College, Salem, Tamilnadu, India¹

P.G. Student, Department of EEE, VMKV Engineering College, Salem, Tamilnadu, India²

ABSTRACT: The principle goal of this research is to reduce Total Harmonics Distortions of this nonlinear load without active or passive filter installations. New generation of CFLs designed for reduce Total Harmonics Distortions with high power factor process and also available in higher price. Simple single switch electronic ballast with passive valley-fill power factor correction with EMI filter is proposed in this project for CFL application. The proposed single-switch ballast circuit is able to achieve zero current switching to maximize the circuit efficiency. A simple feedback circuit with duty ratio control is also proposed to improve the high lamp current crest factor caused by the valley-fill circuit. The output of this project, Total harmonics distortion is minimized, Power factor has been improved and the power loss of the above circuit has been minimized with minimum cost.

KEYWORDS: Total Harmonic Distortion (THD), Electro Magnetic Interference (EMI), EMI Filter, CFL

I. INTRODUCTION

With the global concerns regarding the conservation of the Earth's limited energy resources, the use of compact fluorescent lamps (CFL) or energy-saving light bulbs is being imposed by the governments of a growing list of countries in an attempt to phase out conventional incandescent lamps to reduce energy usage. A single CFL consumes only one-third as much electricity as a standard incandescent lamp when providing the same light output. Hence, by using CFLs, consumers can save a large amount of money in the long-run with the reduced energy cost compared. Due to the size and cost constraint of a CFL, electronic ballast conventionally used in the CFL normally consists of a diode rectifier followed by a half-bridge self-oscillating resonant inverter; the type of resonant circuit that fluorescent lighting ballasts use is usually the typical LC resonant circuit. A major drawback of the aforementioned ballast circuit configuration is that the presence of the large dc-link capacitor limits the conduction time of the input current, which results in poor input power factor. By drawing an input line current with very low power factor, the line current is highly distorted. It is observed that the THD level increases exponentially and is inversely proportional to the power factor. The effect of the poor power factor from CFL on the utility can be illustrated from the following example. Although a single CFL consumes much less power than the incandescent lamp to provide the same luminous intensity, when a large quantity of incandescent lamp is replaced with CFL in the near future, the large amount of current harmonics produced by CFLs will become a severe problem for the utility and the power system network. Hence, it is necessary for the designers of CFL to incorporate power factor correction (PFC) function in its ballast design.

The proposed ballast circuit also has the ability to achieve zero current switching (ZCS) at both turn-on and turn-off of the switch to maximize the power efficiency of the ballast circuit.



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Vol. 5, Issue 6, June 2016

II LITERATURE REVIEW

"Single Phase Converters for Power Factor Correction with Tight Output Voltage Regulation" K. Umamaheswari, V. Venkatachalam IJETA, ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 3, Issue 2, February 2013

The fly back converter type single-stage converter and a half wave rectifier with time-multiplexing control (TMC) for power factor correction is proposed. It has the advantage of better magnetic core utilization and better performance for high power applications. The major portion of the input is transferred to the load through ac-dc conversion. And the part of the input power is delivered to the auxiliary output through the fly back conversion and stored in the capacitor. The voltage ripple of the main output can also be reduced. With TMC the power processes can be achieved by single transformer to reduce the cost and the size of the converter. The simulation result of the proposed converter presents, simplicity, high power factor with low cost and size.

"Simulation of high power factor single state LCC Resonant Inverter" Mohammed Sabah Ul Islam and Dr. S Tara Kalyani International Journal of Conceptions on Electrical & Electronics Engineering Vol. 1, Issue. 2, December 2013; ISSN: 2345 – 9603

This paper presents the simulation of high-power factor (HPF) single-stage inductor-capacitor-capacitor (LCC) resonant inverter. A half-bridge LCC resonant inverter shares switches with a power factor- correction circuit to form single stage. The proposed single stage LCC resonant inverter can achieve almost unity power factor and ripple-free input current, and can also realize zero-voltage-switching by operating the witches above the resonant frequency. The simulated result is compared with the results of conventional inverter, LLC resonant inverter and Z-source inverter. Among all these results, LCC resonant inverter has the high power factor value which is almost unity. Thus, the proposed single-stage inverter provides HPF to the utility line and also achieves circuit simplicity, low cost, and high reliability.

From the above literature review following problems are identified

- The line current drawn from the CFL produce a large amount of unwanted harmonics that results in very poor input power factor;
- The dimming performance of a CFL with conventional incandescent lamp dimmers is very poor.
- The performance of the CFL depends on the design of the electronic ballast circuit that is located at the base of each CFL.
- These problems are prevented by using my proposed method.

III. PROPOSED METHOD

Incandescent lamps are now being gradually replaced by Compact Fluorescent Lamps (CFLs) as CFLs consume less power to produce the same light output and its lifetime is much longer than that of an incandescent lamp. A simple single switch electronic ballast with passive valley-fill power factor correction is proposed in this paper for CFL application. The single-switch ballast circuit is able to achieve zero current switching to maximize the circuit efficiency.

A simple feedback circuit with duty ratio control is also proposed to improve the high lamp current crest factor caused by the valley-fill circuit. Detailed descriptions and analysis of the circuit operating principles are provided in this paper.

The propose method have a new control circuit that enables the lamp to maintain high power factor throughout the majority of the dimming range. In the proposed control scheme, the dimmer ANN closed loop is fed-forward to the control circuit. The controller then determines the proper duty cycle based on the ANN closed loop to facilitate the desired dimming operation. This novel control circuit was first implemented using analog circuity.



(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 6, June 2016

BLOCK DIAGRAM

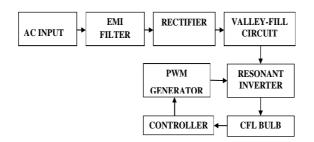


Fig 1 Proposed method Block Diagram

BLOCK DIAGRAM EXPLANATION

EMI FILTER

An EMI filter, or electromagnetic interference filter, is an electronic passive device which is used in order to suppress conducted interference that is present on a signal or power line.

RECTIFIER

A rectifier is an electrical device that converts alternating current (AC), which periodically reverses direction, to direct current (DC), which flows in only one direction. The process is known as rectification. Physically, rectifiers take a number of forms, including vacuum tube diodes, mercury-arc valves, copper and selenium oxide rectifiers, semiconductor diodes, silicon-controlled rectifiers and other silicon-based semiconductor switches.

VALLY FILL CIRCUIT

A valley-fill circuit is a type of passive power factor correction (PFC) circuit. For purposes of illustration, a basic full-wave diode-bridge rectifier is shown in the first stage, which converts the AC input voltage to a DC voltage.

When the AC voltage is applied, the rectified line voltage is applied across C1 and C2, as they are both charged via D3 and R1, until C1 and C2 are each charged up to approximately half of the peak line voltage. When the line voltage falls below the peak, into the "valley" phase, Vout begins to fall toward half of the peak line voltage. At this point, C1 and C2 begin to discharge into the load at Volt, via D1 and D2 respectively. R1 is needed to prevent a large in-rush current and electromagnetic interference.

ANN

The term neural network was traditionally used to refer to a network or circuit of biological neurons. The modern usage of the term often refers to artificial neural networks, which are composed of artificial neurons or nodes. Thus the term has two distinct usages.

Biological neural networks are made up of real biological neurons that are connected or functionally related in the peripheral nervous system or the central nervous system. In the field of neuroscience, they are often identified as groups of neurons that perform a specific physiological function in laboratory analysis.

Artificial neural networks are composed of interconnecting artificial neurons (programming constructs that mimic the properties of biological neurons). Artificial neural networks may either be used to gain an understanding of biological neural networks, or for solving artificial intelligence problems without necessarily creating a model of a real biological system. The real, biological nervous system is highly complex: artificial neural network algorithms attempt to abstract this complexity and focus on what may hypothetically matter most from an information processing point of



(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 6, June 2016

view. Good performance (e.g. as measured by good predictive ability, low generalization error), or performance mimicking animal or human error patterns, can then be used as one source of evidence towards supporting the hypothesis that the abstraction really captured something important from the point of view of information processing in the brain. Another incentive for these abstractions is to reduce the amount of computation required to simulate artificial neural networks, so as to allow one to experiment with larger networks and train them on larger data sets.

PWM

Pulse-width modulation (PWM), or pulse-duration modulation (PDM), is a commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches.

The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast pace. The longer the switch is on compared to the off periods, the higher the power supplied to the load is.

The PWM switching frequency has to be much faster than what would affect the load, which is to say the device that uses the power. Typically switchings have to be done several times a minute in an electric stove, 120 Hz in a lamp dimmer, from few kilohertz (kHz) to tens of kHz for a motor drive and well into the tens or hundreds of kHz in audio amplifiers and computer power supplies.

The term duty cycle describes the proportion of 'on' time to the regular interval or 'period' of time; a low duty cycle corresponds to low power, because the power is off for most of the time. Duty cycle is expressed in percent, 100% being fully on.

The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on, there is almost no voltage drop across the switch. Power loss, being the product of voltage and current, is thus in both cases close to zero. PWM also works well with digital controls, which, because of their on/off nature, can easily set the needed duty cycle.

In Pulse Width Modulation (PWM) mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the CCPx pin is multiplexed with the PORT data latch, the corresponding TRIS bit must be cleared to make the CCPx pin an output.

IV. CIRCUIT DIAGRAM

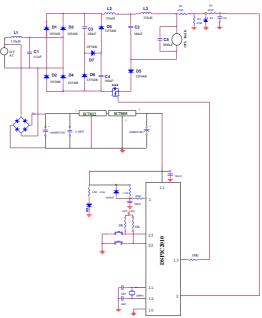


Fig 3 Circuit Diagram



(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 6, June 2016

Stage 1: t0 < t < t1. When Vg (the gate signal to M1) is high, M1 is on. *i*in flows from the output of the valley-fill circuit to *L*in, the resonant circuit, *D*4, and *M*1. The current (*i*ds)flowing through *M*1 is simply equal to *i*in.

Stage 2: t1 < t < t2. *M*1 is still on. Meanwhile, diode *D*4should turn off so that *i*in returns to zero before the switch turn off to minimize the MOSFET turn off switching loss. In this stage, the current flowing through *M*1 is equal to zero.

Stage 3: t2 < t < T s. *Vg* goes to zero, and *M*1 turns off. Once *M*1 turns off, the voltage across *M*1 starts to increase due to the presence of the drain-to-source capacitor of *M*1. It can be seen that the voltage stress across the MOSFET is a function of vrect and θ , where ω is the angular switching frequency; vrect is the voltage across the valley-fill circuit and is assumed to be constant (*V*rect) within one switching cycle.

V. RESULT AND DISCUSSIONS

This paper work on harmonic interactions in nonlinear loads, especially CFLs with electronic ballast. There for a novel filter less method for harmonic suppression between groups of same loads has proposed. Experimental measurements will give to evaluate the attenuation effect between different individual lamps.

Sl.No	Description	Conventional method without feedback	Proposed method with feedback
01	Total Harmonics Distortion	0.7%	0.2%
02	Power consumption	15W	13.5W
03	Power Factor	0.900	0.960
04	Power loss	25%	10%

Table 1 Result

The above table shows the total harmonic distortion, Power Consumption, Power factor and Power Loss in both conventional and proposed method .In all the cases the proposed method results shows high accuracy and efficiency. Based upon the experimental results the proposed method gives the better performance.

INPUT VOLTAGE

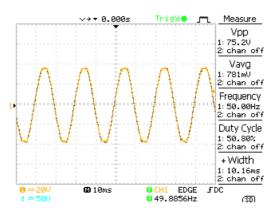


Fig 4 Input voltage to the Proposed Circuit

In the fig 4 the input voltage in the proposed method is shown for better understanding of the method almost 24 V is applied to the proposed system. The loss less sinusoidal waveform shows the rate of loss is low at the same time the ripples in the input voltage is also low.



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Vol. 5, Issue 6, June 2016

GATE PULSE

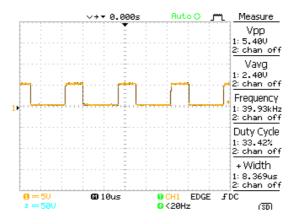
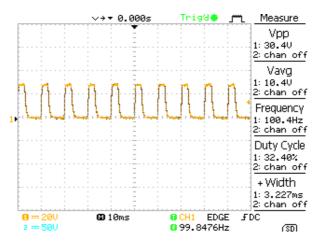


Fig 5 Gate Pulse to the proposed method

The Gate Pulse also be the factor effects the Performance of the Device. The Gate pulse which is used for Switching operation to drive the MOSFET Switch. It indicate the pulse generates at 400 Hz switching frequency and it works at 27% Duty cycle. In this duty we can control voltage at constant by varying duty cycle.



CFL OUTPUT VOLTAGE WITHOUT HARMONICS

Fig 6 Output Voltage

The output voltage of the CFL is shown in the fig ,If the harmonics occur in the output voltage it fails the device performance in lower state .The output closed loop system voltage waveform maintain the constant output voltage at 24V at any variations in input voltage and harmonics.



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Vol. 5, Issue 6, June 2016

VI. CONCLUSION

Single-switch has been presented in this paper for CFLs to improve the poor power factor performance in the conventional ballast design. A passive valley-fill circuit was used as the Total Harmonics distortion, Power factor improvement and reduces the power loss in the proposed ballast to form a high-power-factor single-switch ballast power circuit. To improve the lamp illumination, a simple feedback circuit to control the "valley-fill" low-frequency envelope imposed on the lamp current by adjusting the duty ratio of the switch was presented in proto type kit. The output of the above proposed method, Total harmonics distortion is minimized, Power factor has been improved and the power loss of the above circuit has been minimized.

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